FIG. 1

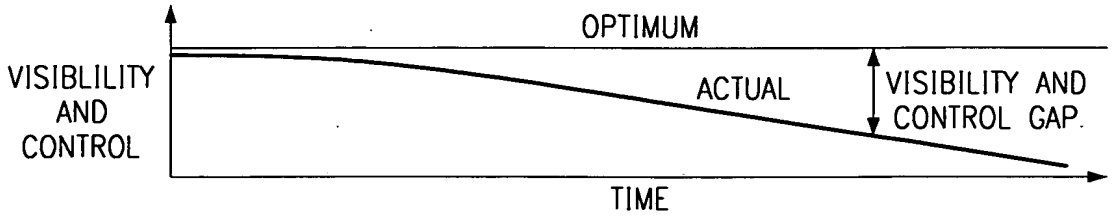
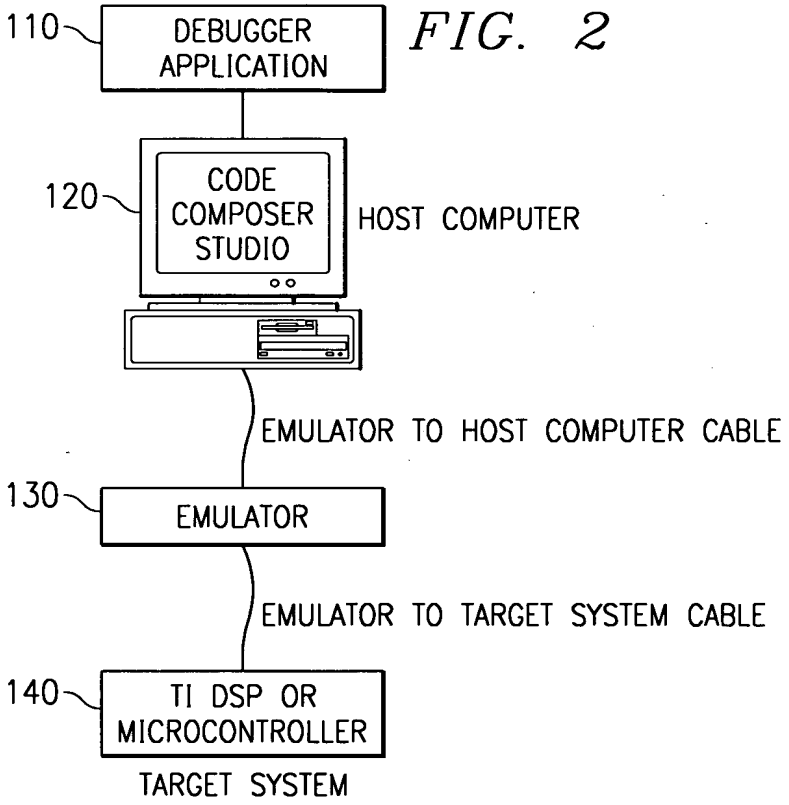


FIG. 2



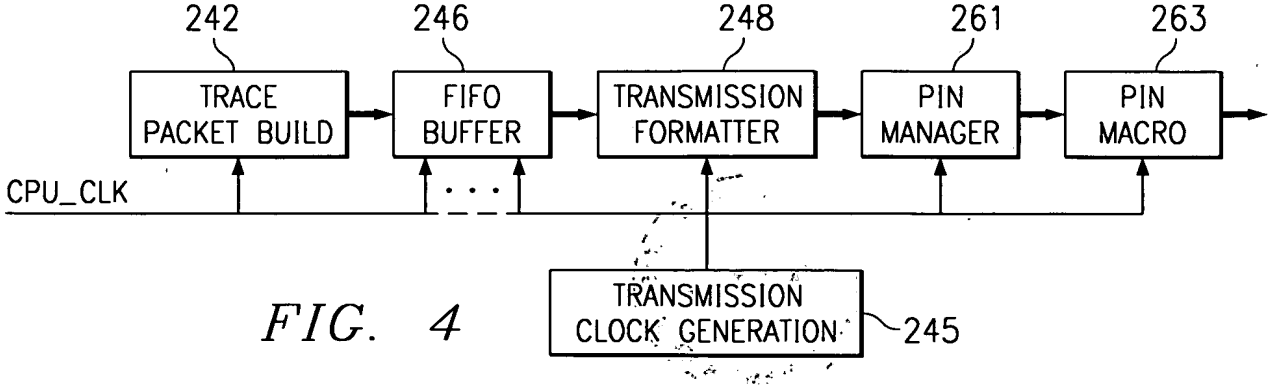


FIG. 4

FIG. 3

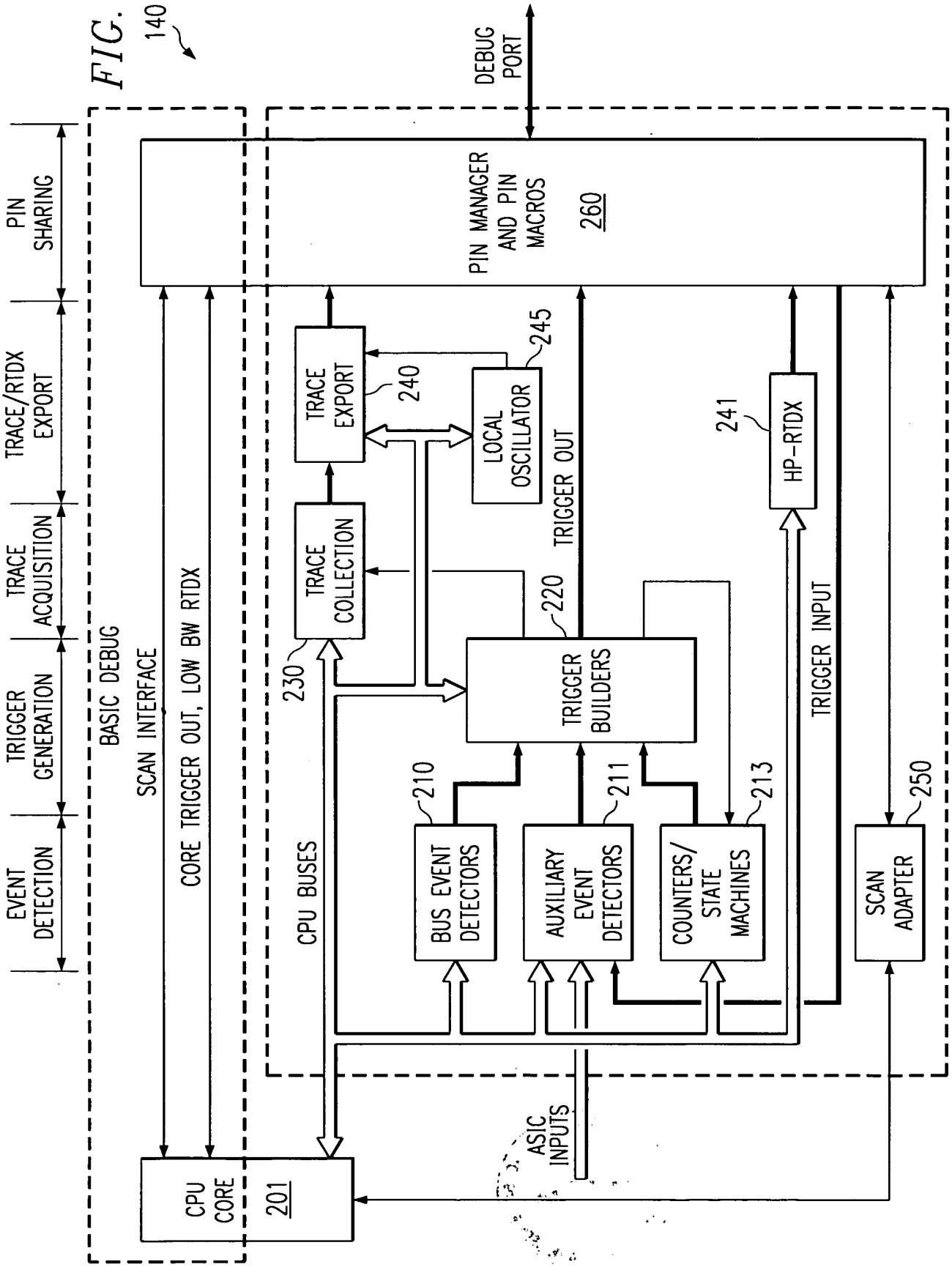

140
DEBUG PORT
PIN SHARING
TRACE/RTDX EXPORT
TRACE ACQUISITION
TRIGGER GENERATION
EVENT DETECTION
BASIC DEBUG
SCAN INTERFACE
CORE TRIGGER OUT, LOW BW RTDX
PIN MANAGER AND PIN MACROS
260
TRACE EXPORT
240
LOCAL OSCILLATOR
245
TRACE COLLECTION
230
TRIGGER OUT
220
TRIGGER BUILDERS
HP-RTDX
241
TRIGGER INPUT
CPU BUSES
BUS EVENT DETECTORS
210
AUXILIARY EVENT DETECTORS
211
COUNTERS/ STATE MACHINES
213
SCAN ADAPTER
250
ASIC INPUTS
CPU CORE
201

FIG. 5

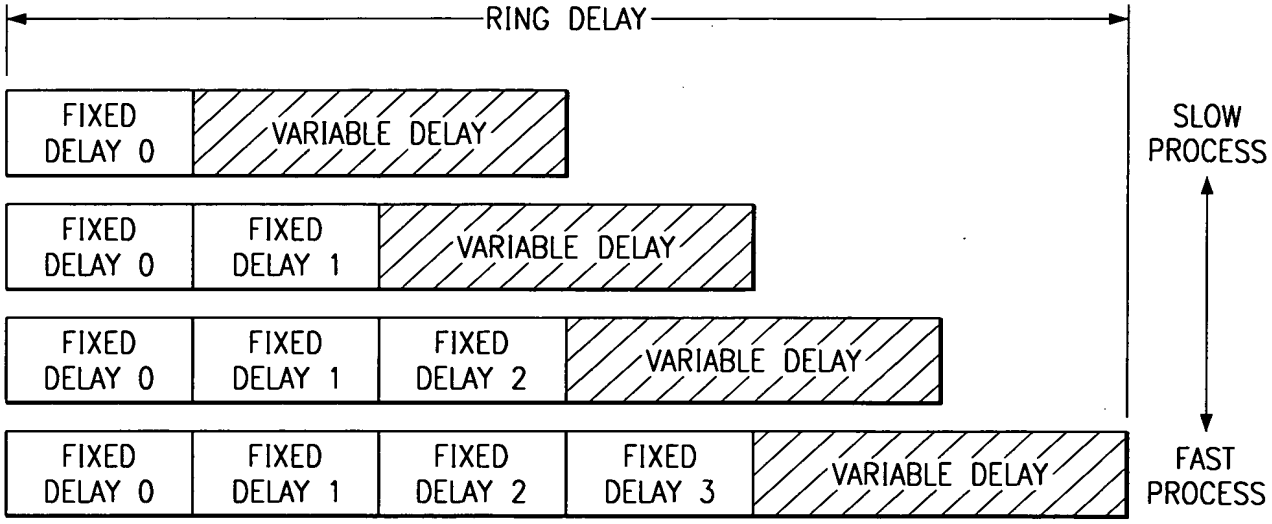
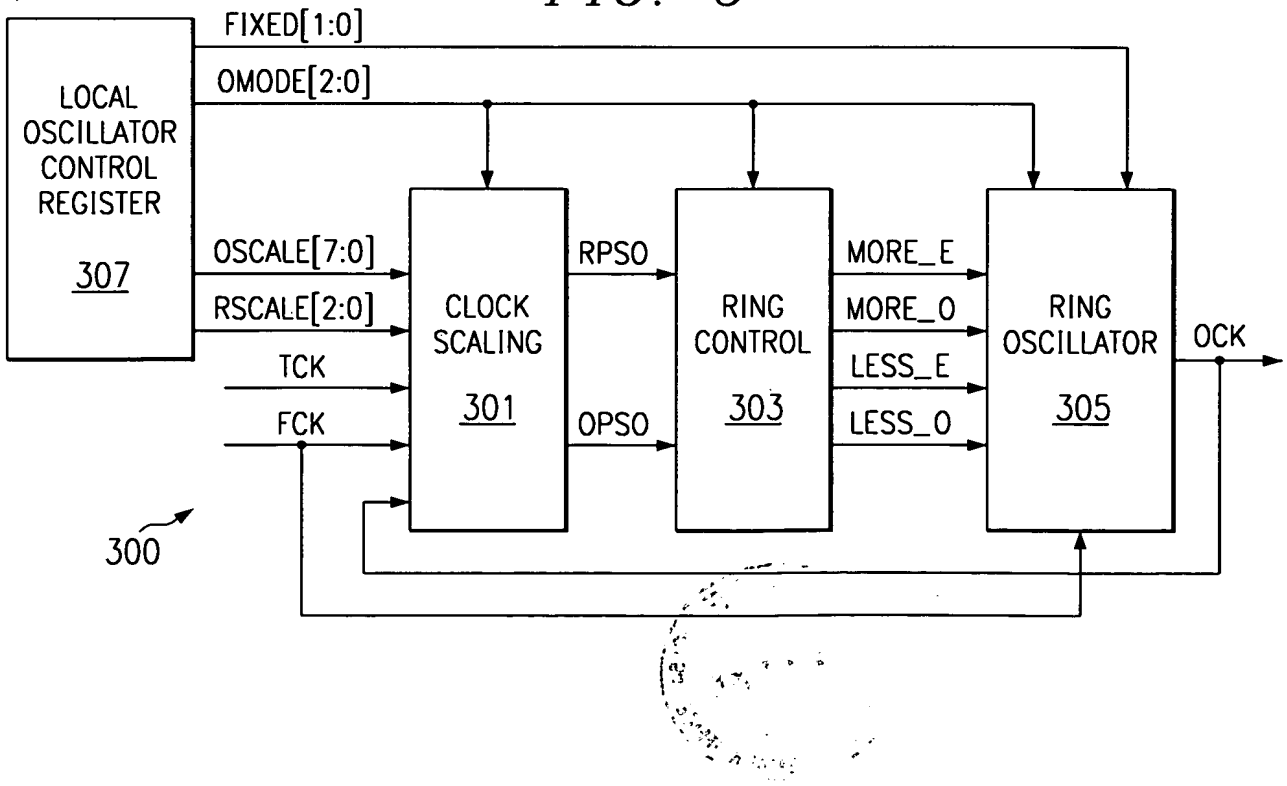

RING DELAY
FIXED DELAY 0
VARIABLE DELAY
FIXED DELAY 0
FIXED DELAY 1
VARIABLE DELAY
FIXED DELAY 0
FIXED DELAY 1
FIXED DELAY 2
VARIABLE DELAY
FIXED DELAY 0
FIXED DELAY 1
FIXED DELAY 2
FIXED DELAY 3
VARIABLE DELAY
SLOW PROCESS
FAST PROCESS

FIG. 6


LOCAL OSCILLATOR CONTROL REGISTER
307
FIXED[1:0]
OMODE[2:0]
OSCALE[7:0]
RSCALE[2:0]
TCK
FCK
CLOCK SCALING
301
RPSO
OPSO
RING CONTROL
303
MORE_E
MORE_O
LESS_E
LESS_O
RING OSCILLATOR
305
OCK
300

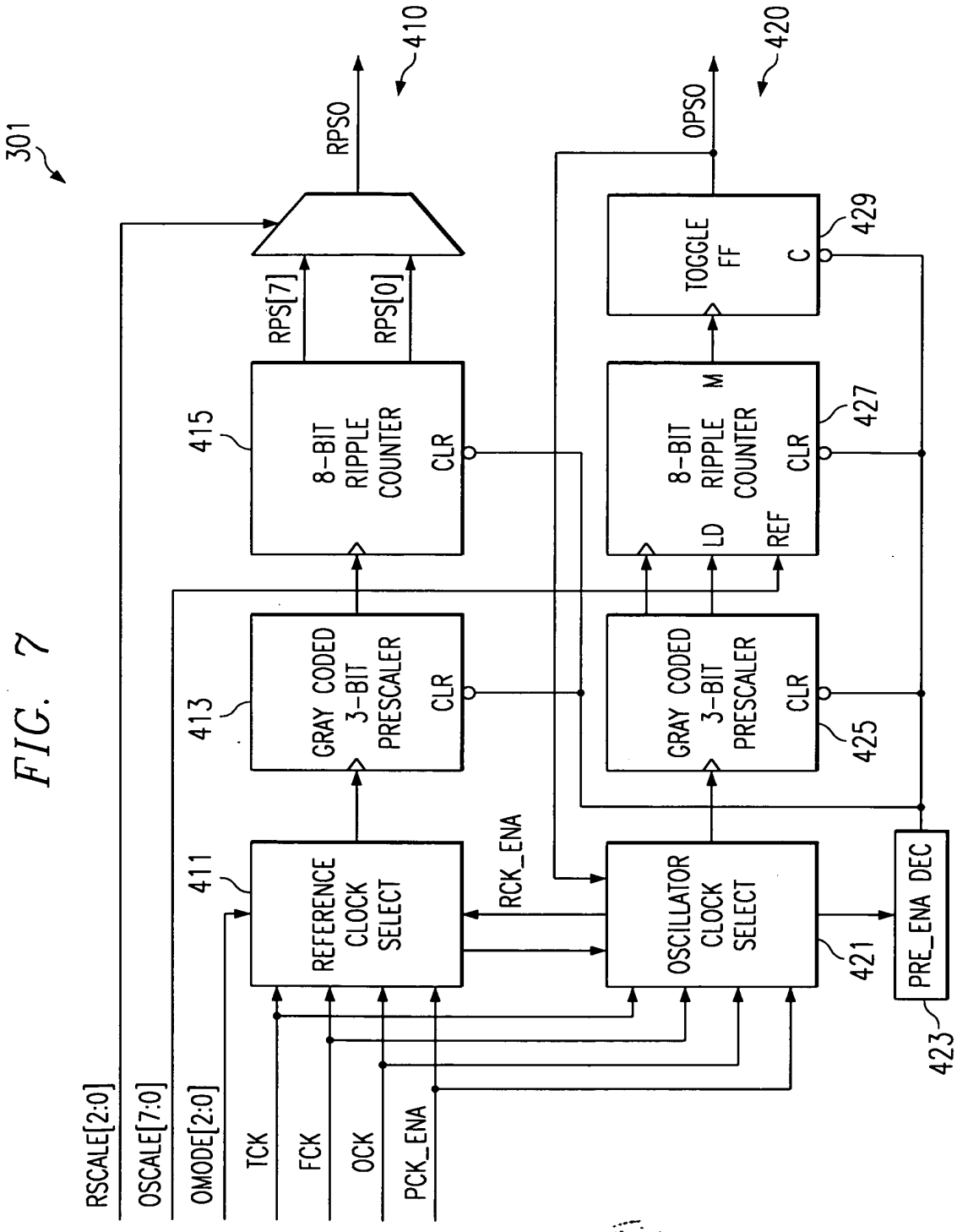

301
410
RPSO
420
OPSO
RPS[7]
RPS[0]
415
8-BIT RIPPLE COUNTER
CLR
TOGGLE FF
C
429
M
427
LD
REF
413
GRAY CODED 3-BIT PRESCALER
425
411
REFERENCE CLOCK SELECT
RCK_ENA
OSCILLATOR CLOCK SELECT
421
PRE_ENA DEC
423
RSCALE[2:0]
OSCALE[7:0]
OMODE[2:0]
TCK
FCK
OCK
PCK_ENA

FIG. 7

FIG. 8

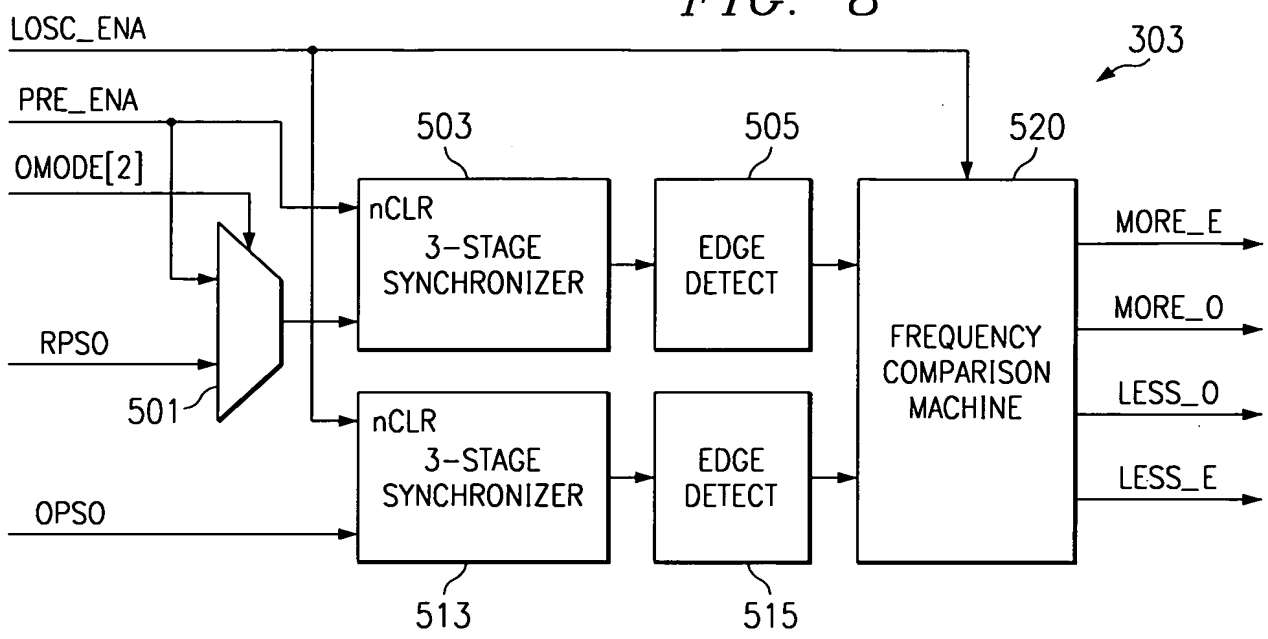
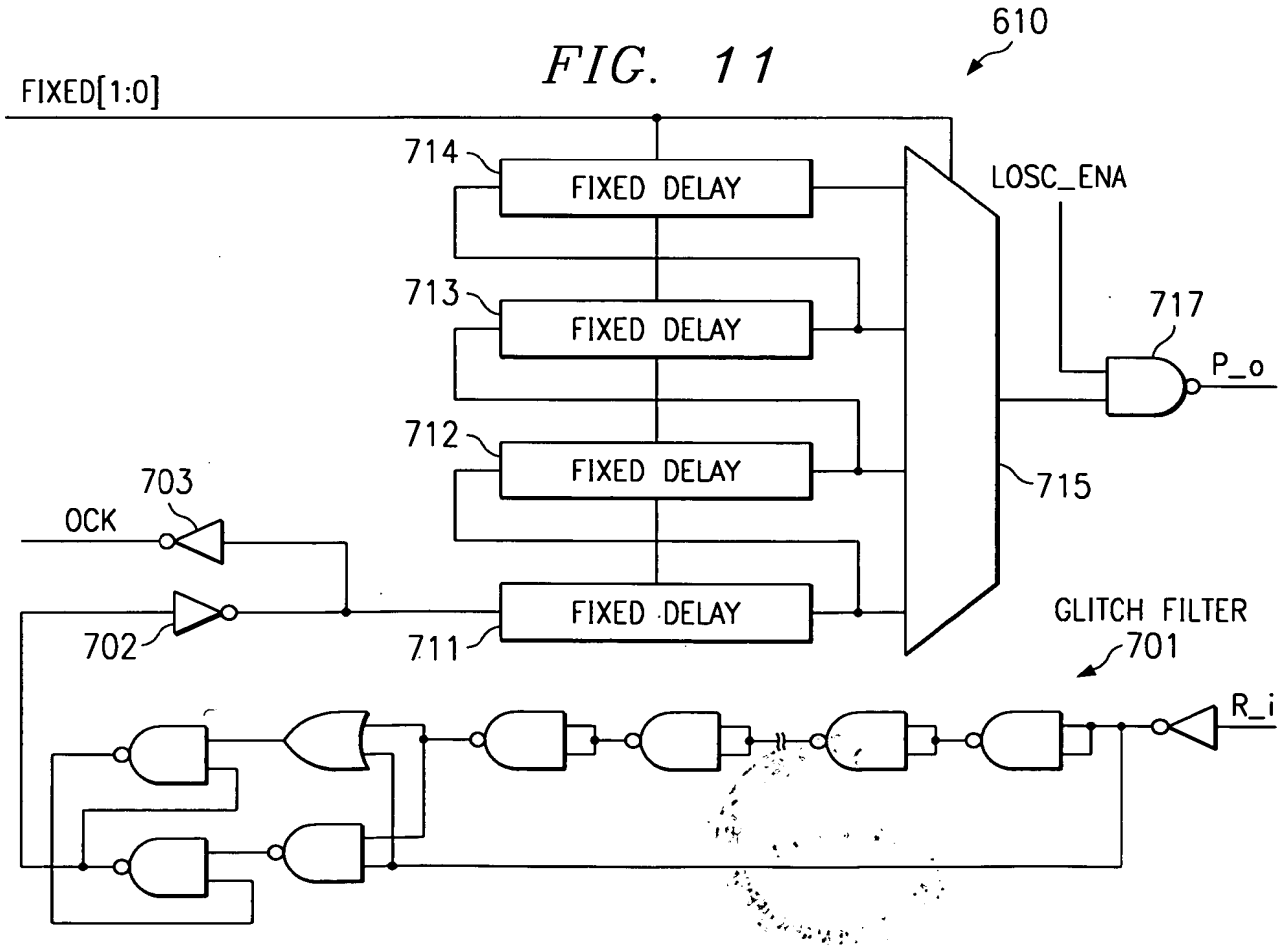
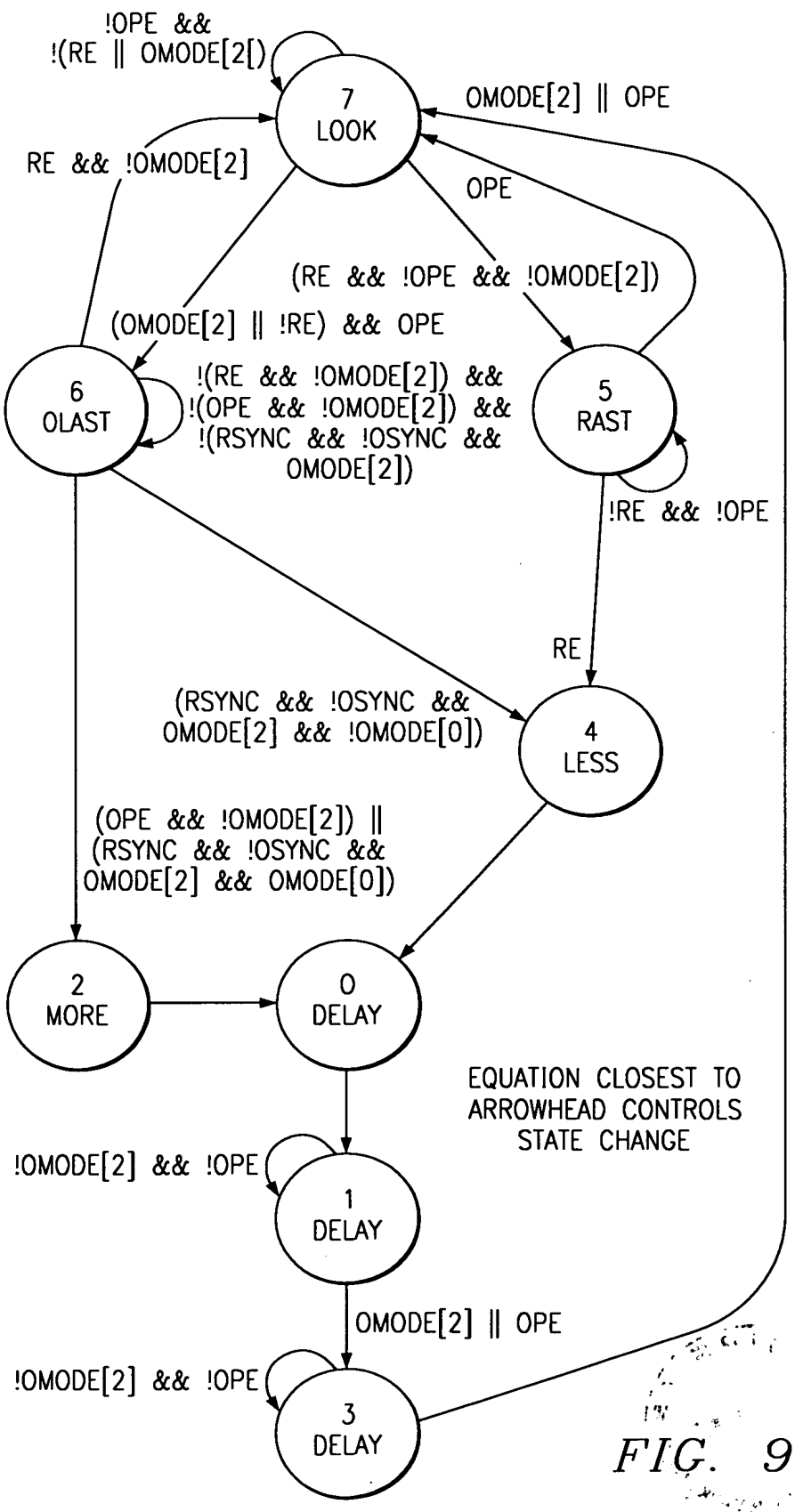

LOSC_ENA
303
PRE_ENA
503
505
520
OMODE[2]
nCLR
3-STAGE
SYNCHRONIZER
EDGE
DETECT
MORE_E
MORE_O
RPSO
FREQUENCY
COMPARISON
MACHINE
LESS_O
501
nCLR
3-STAGE
SYNCHRONIZER
EDGE
DETECT
LESS_E
OPSO
513
515

FIG. 11


610
FIXED[1:0]
714
FIXED DELAY
LOSC_ENA
713
FIXED DELAY
717
P_o
712
FIXED DELAY
703
715
OCK
FIXED DELAY
GLITCH FILTER
702
711
701
R_i



SIGNAL DEFINITION

RE – REFERENCE EDGE
OPE – OSCILLATOR POSITIVE EDGE
RSYNC – REFERENCE INPUT SYNCHRONIZED
OSYNC – OSCILLATOR INPUT SYNCHRONIZED

STATE FUNCTION (OMODE[2] == FALSE)

0 – DELAY OR START STATE
1 – WAIT FOR OSCILLATOR PRESCALER POSITIVE EDGE
2 – OSCILLATOR FASTER THAN REFERENCE
3 – WAIT FOR OSCILLATOR PRESCALER CARRY EDGE
4 – REFERENCE FASTER THAN OSCILLATOR
5 – REFERENCE EDGE
6 – OSCILLATOR EDGE
7 – WAIT FOR OSCILLATOR OR REFERENCE EDGE

STATE FUNCTION (OMODE[2] == TRUE)

0 – WAIT FOR PRE_ENA (RSYNC)
1 – DELAY
2 – INCREASE RING DELAY
3 – DELAY
4 – DECREASE RING DELAY
5 – ILLEGAL
6 – END OF MEASUREMENT, WAIT FOR OPSO TO GO TO ZERO (!OSYNC) AND RSYNC TO GO TO A ONE (PRE_ENA)
7 – OPSO TO GO TO ONE

LOSC_ENA ASYNCHRONOUSLY ASSIGNS THE STATE TO 0 WHEN A LOGIC 0

FIG. 9

FIG. 10

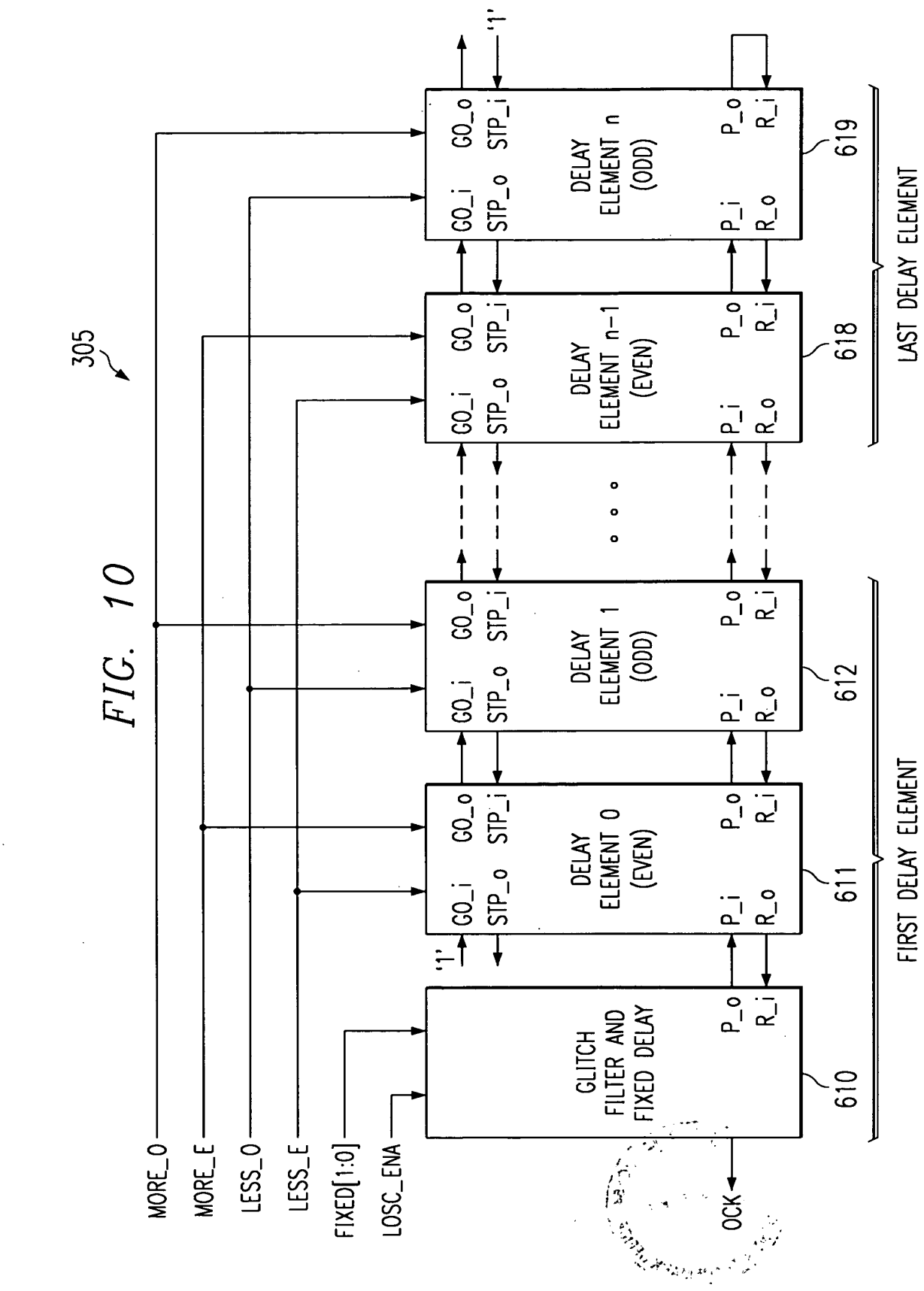

305
MORE_O
MORE_E
LESS_O
LESS_E
FIXED[1:0]
LOSC_ENA
OCK
GLITCH FILTER AND FIXED DELAY
610
DELAY ELEMENT 0 (EVEN)
611
DELAY ELEMENT 1 (ODD)
612
DELAY ELEMENT n-1 (EVEN)
618
DELAY ELEMENT n (ODD)
619
FIRST DELAY ELEMENT
LAST DELAY ELEMENT
'1'
'1'
GO_i
GO_o
STP_i
STP_o
P_i
P_o
R_i
R_o

FIG. 12

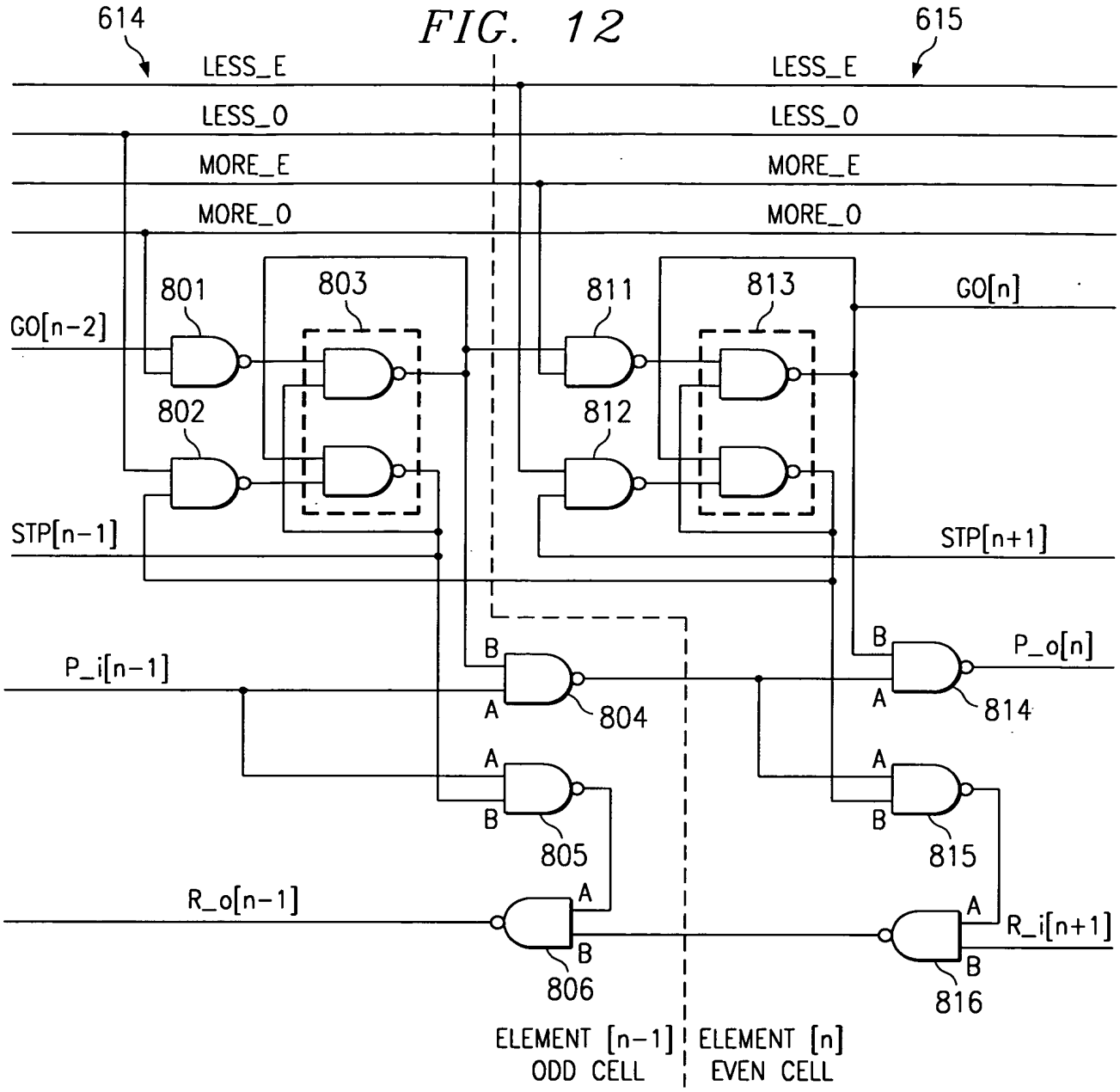
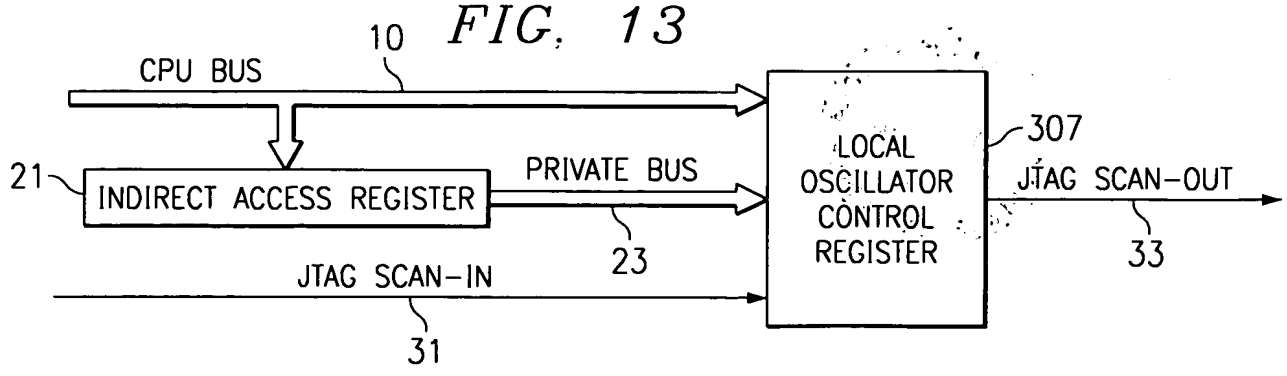

614
615
LESS_E
LESS_O
MORE_E
MORE_O
801
802
803
811
812
813
GO[n-2]
GO[n]
STP[n-1]
STP[n+1]
P_i[n-1]
P_o[n]
804
814
805
815
R_o[n-1]
R_i[n+1]
806
816
ELEMENT [n-1]
ODD CELL
ELEMENT [n]
EVEN CELL

FIG. 13


10
CPU BUS
21
INDIRECT ACCESS REGISTER
PRIVATE BUS
23
JTAG SCAN-IN
31
LOCAL
OSCILLATOR
CONTROL
REGISTER
307
JTAG SCAN-OUT
33